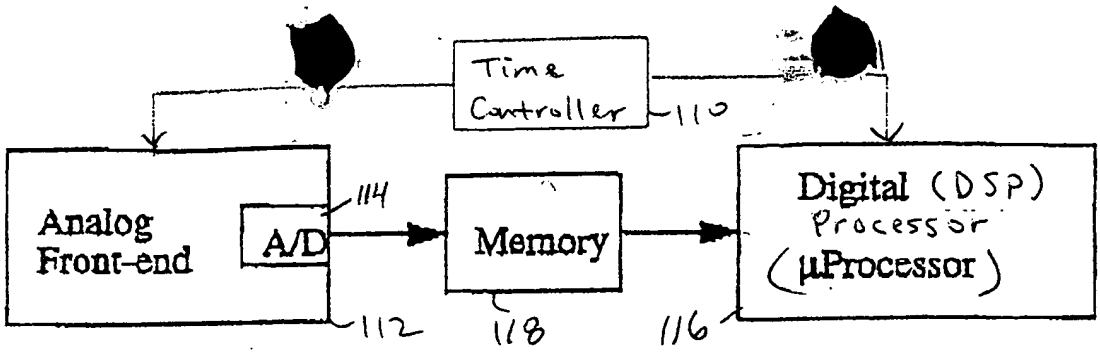

Figure 1: Receiver Block Diagram

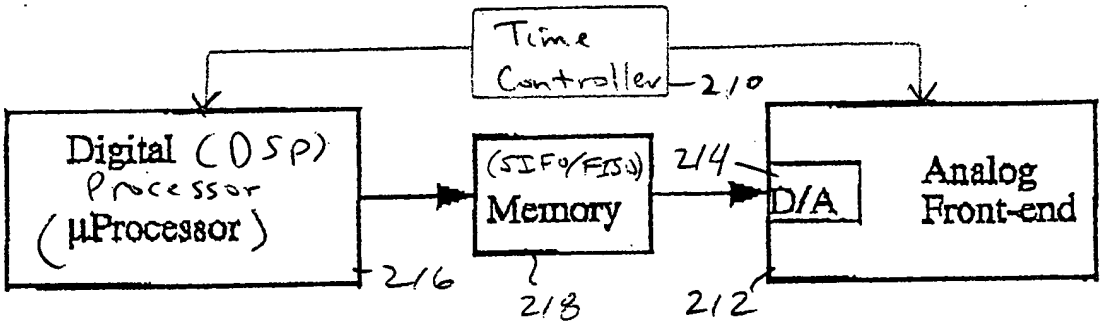

Figure 2: Transmitter Block Diagram

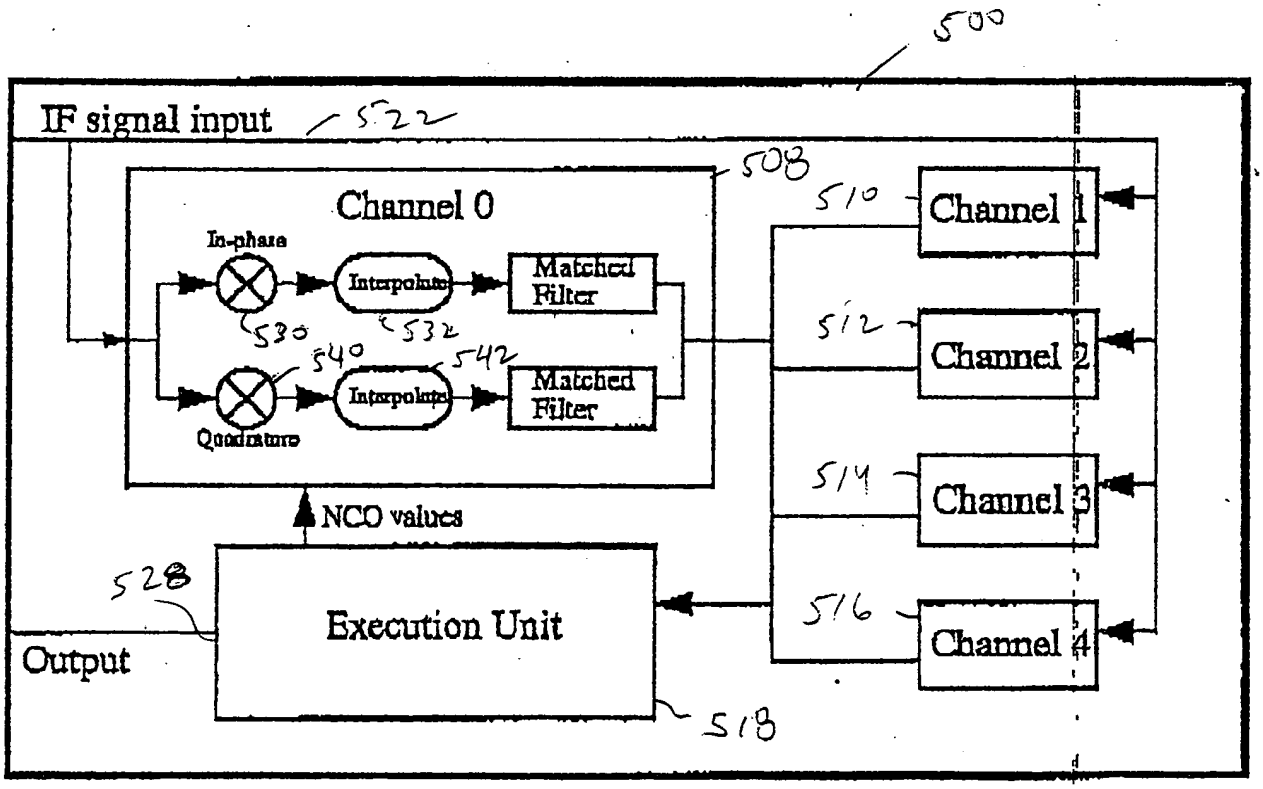

Figure 5 **Synchronizer Architecture**

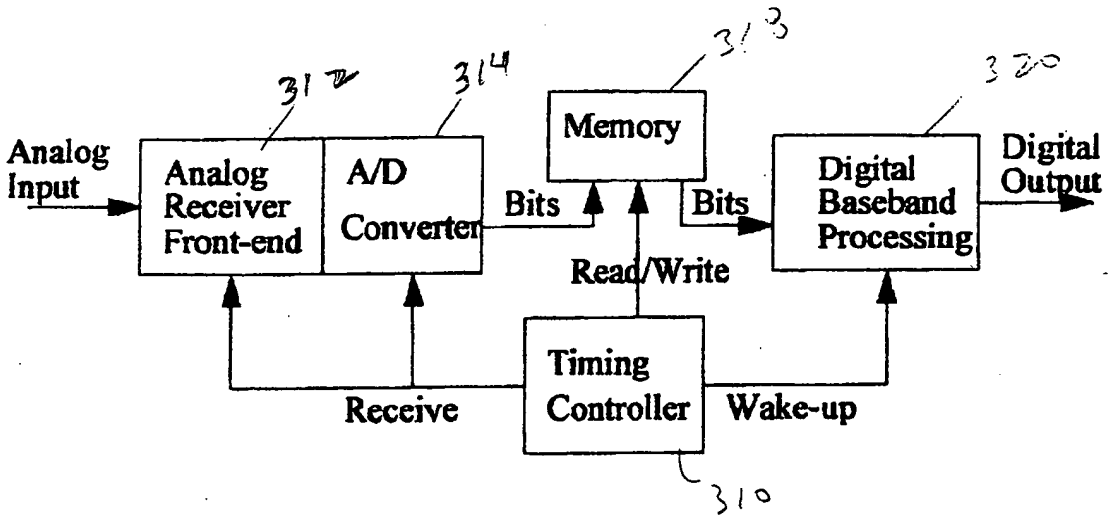

Figure 3 Time-interleaved receiver architecture. The timing controller regulates the receiver operation between the analog receiver front-end circuitry and the baseband processing. It also controls the memory in performing time-interleaving read/write operations.

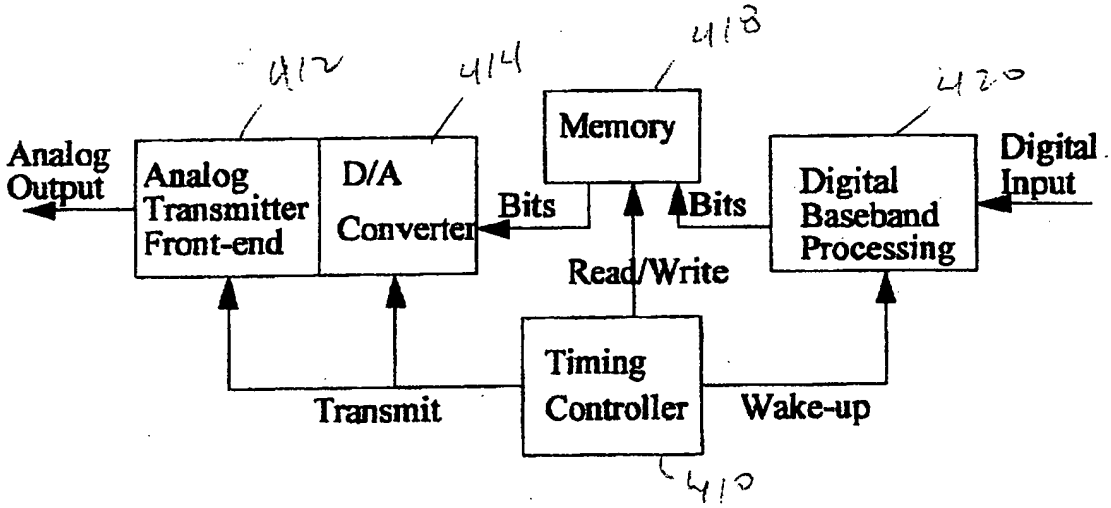

Figure 4. Time-interleaved transmitter architecture. The timing controller regulates the transmitter operation between the analog transmitter front-end circuitry and the baseband processing. It also regulates the memory in performing time-interleaving read/write operations.

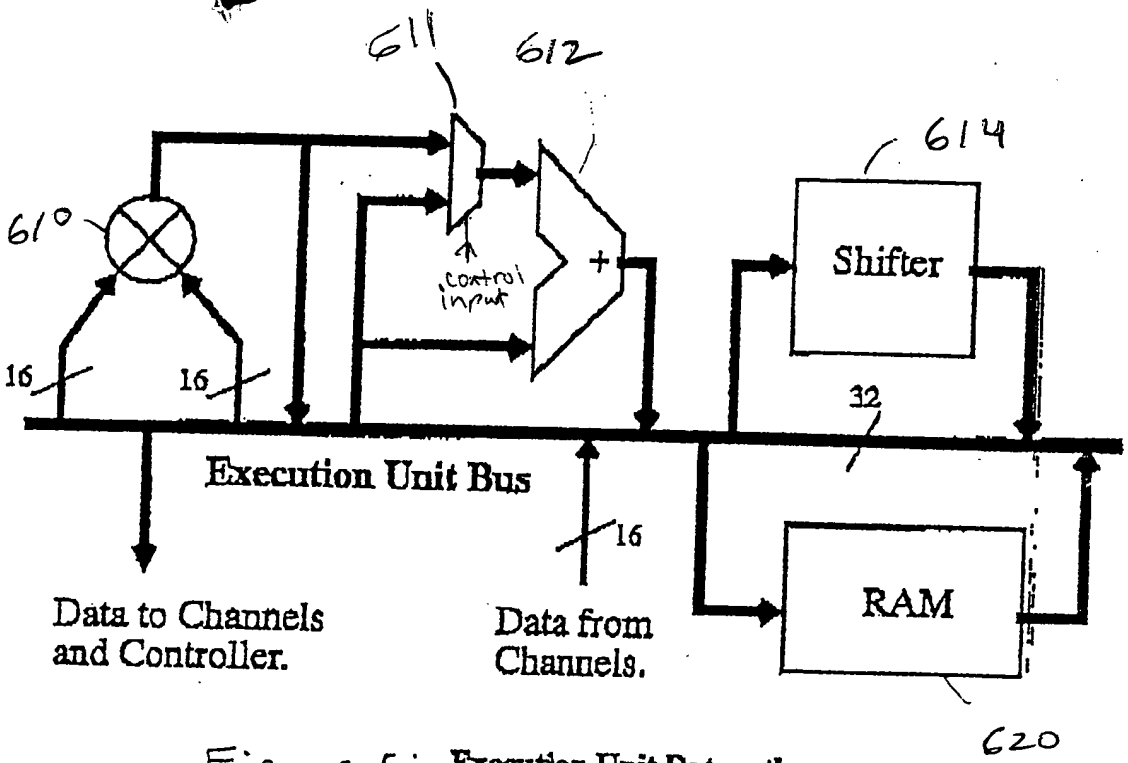

Figure 6: Execution Unit Datapath

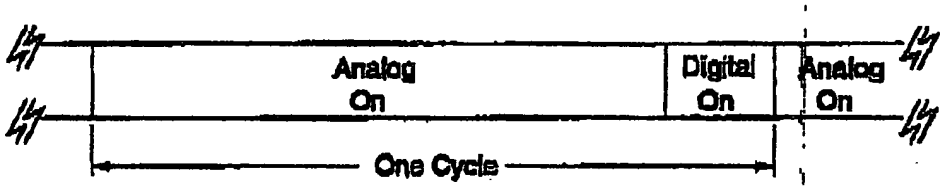

Fig. 7a

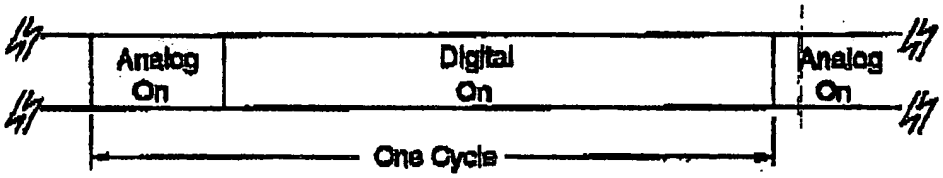

Fig. 7b

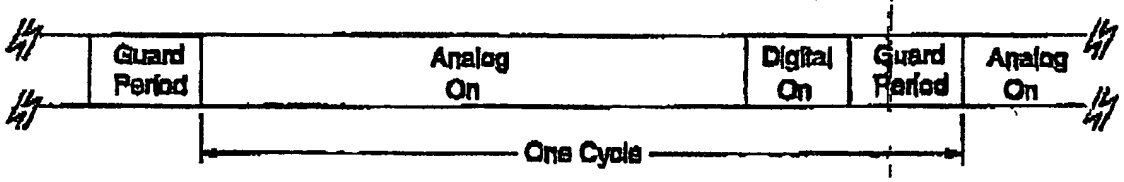

Fig. 7c

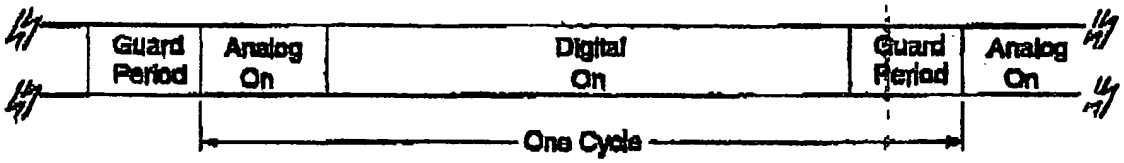

Fig. 7d